Amendments to the claims

1. (Presently Amended) A hetero-interface field effect transistor comprising:

a substrate; and

a layered QW structure including at least a barrier layer in contact with a channel layer in contact with an underlying layer grown to provide a cation-polarity layered structure including at least said **[[a]]** barrier layer and said **[[a]]** channel layer wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0 \leq x \leq 0.30$, and wherein said channel layer includes polarization induced charge.

2. (Original) The hetero-interface field-effect transistor according to claim 1 wherein said barrier layer includes $In_{0.17}Al_{0.83}N$

3. (Original) The hetero-interface field-effect transistor according to claim 2 wherein said channel layer includes GaN

4. (Presently Amended) A **[[The]]** hetero-interface field-effect transistor ~~according to claim 2~~ comprising:

a substrate; and

a cation-polarity layered structure including at least a barrier layer and a channel layer wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0 \leq x \leq 0.30$, wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range to provide compressive strain in said channel layer ~~of about $0<y\leq 1$~~.

5. (Original) The hetero-interface field-effect transistor according to claim 1 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0 \leq x < 0.17$.

6. (Original) The hetero-interface field-effect transistor according to claim 5 wherein said channel layer includes GaN

7. (Original) The hetero-interface field-effect transistor according to claim 5 wherein said channel layer includes $In_yGa_{1-y}N$ ($0<y\leq 1$).

8. (Original) The hetero-interface field-effect transistor according to claim 1 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0.17<x\leq 0.25$

9. (Original) The hetero-interface field-effect transistor according to claim 8 wherein said channel layer includes GaN.

10. (Original) The hetero-interface field-effect transistor according to claim 8 wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range of about $0<y\leq 1$.

11. (Original) The hetero-interface field-effect transistor according to claim 1 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0.25<x\leq 0.30$.

12. (Original) The hetero-interface field-effect transistor according to claim 11 wherein said channel layer includes $In_yGa_{1-y}N$, x being in the range of about $0<y\leq 1$.

13. (Presently Amended) A hetero-interface field effect transistor comprising:

a substrate; and

a layered QW structure including at least a barrier layer <u>in contact with</u> **[[and]]** a channel layer ~~providing~~ <u>in contact with a layer grown to provide cation polarity of said barrier layer and said channel layer, said channel layer exhibiting polarization induced charge having</u> the total two dimensional electron gas density of above $n_{total} = 1.1 \times 10^{13}$ cm^{-2}.

Claims 14 – 21 cancelled

22. (Presently Amended) A method for fabricating a hetero-interface field effect transistor comprising:

providing a substrate;

depositing sequentially two layers on an underlying layer grown to provide a cation-polarity layered structure; and

fabricating a layered QW structure from said cation polarity layered structure including at least a barrier layer and a channel layer providing the total two dimensional electron gas density of above $n_{total} = 1.1 \times 10^{13}\,cm^{-2}$.

23. (Presently Amended) A method for fabricating a hetero-interface field effect transistor comprising:

providing a substrate;

depositing sequentially two layers on an underlying layer grown to provide a cation-polarity layered structure; and

fabricating a layered QW structure from said cation polarity layered structure including at least a barrier layer and a channel layer wherein barrier layer includes $In_xAl_{1-x}N$ where $0 \leq x \leq 0.30$.

Claim 24 cancelled

Claim 25 cancelled

26. (Presently Amended) An electronic device utilizing a hetero-interface field effect transistor comprising a substrate, and a layered quantum well structure including at least **[[a]]**an InAlN barrier layer and a channel layer providing a polarization-induced charge and enabling open channel drain current of above 1.5 A/mm.

27. (Original) The hetero-interface field-effect transistor according to claim 26 wherein said channel layer includes GaN.

28. (Original) The hetero-interface field-effect transistor according to claim 26 wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range of about $0<y\leq 1$.

29. (Original) The hetero-interface field-effect transistor according to claim 26 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0\leq x<0.17$.

30. (Original) The hetero-interface field-effect transistor according to claim 29 wherein said channel layer includes GaN.

31. (New) The hetero-interface field-effect transistor according to claim 13 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0\leq x<0.17$.

32. (New) The hetero-interface field-effect transistor according to claim 31 wherein said channel layer includes GaN

33. (New) The hetero-interface field-effect transistor according to claim 31 wherein said channel layer includes $In_yGa_{1-y}N$ ($0<y\leq 1$).

34. (New) The hetero-interface field-effect transistor according to claim 13 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0.17<x\leq 0.25$

35. (New) The hetero-interface field-effect transistor according to claim 34 wherein said channel layer includes GaN.

36. (New) The hetero-interface field-effect transistor according to claim 34 wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range of about $0<y\leq 1$.

37. (New) A hetero-interface field effect transistor comprising:

a substrate; and

a cation-polarity layered structure including at least a barrier layer and a channel layer wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0 \leq x \leq 0.30$, and wherein said channel layer includes polarization-induced charge and exhibits compressive strain.

38. (New) The hetero-interface field-effect transistor according to claim 37 wherein said barrier layer includes $In_xAl_{1-x}N$, x being in the range of about $0.25 < x \leq 0.30$.

39. (New) The hetero-interface field-effect transistor according to claim 37 wherein said channel layer includes $In_{0.10}Ga_{0.90}N$.

40. (New) The method for fabricating hetero-interface field-effect transistor according to claim 22 or 23 wherein said channel layer includes GaN.

41. (New) The method for fabricating hetero-interface field-effect transistor according to claim 22 or 23 wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range of about $0 < y \leq 1$.

42. (New) The method for fabricating hetero-interface field-effect transistor according to claim 22 or 23 wherein said channel layer includes $In_yGa_{1-y}N$, y being in the range to provide compressive strain in said channel layer.